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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/737,119	12/17/2003	Hiroshi Kuroda	XA-10006	5995

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EXAMINER	
NGUYEN, DILINH P	

ART UNIT	PAPER NUMBER
2814	

NOTIFICATION DATE	DELIVERY MODE
03/19/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/737,119	KURODA ET AL.	
	Examiner	Art Unit	
	DILINH NGUYEN	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 December 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 6-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 6-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Remark

Claims 1-3 and 6-20 are pending in the application. Claims 4-5 have been canceled by Applicants.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 14-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The citation of "wherein the bonding terminals include an external interface terminal electrically connected outside of a system comprising the memory chip and the microcomputer chip, and an internal interface terminal electrically connected with the memory chip" (claim 14) renders the claim indefinite.

It is not clear where and how an external interface terminal electrically connected outside of a system comprising the memory chip and the microcomputer chip, and an internal interface terminal electrically connected with the memory chip.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3 and 6-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hiroaki et al. (JP. 2001-291821) in view of Katagiri et al. (U.S. Pat. 6841881).

Regarding claims 1 and 6, Hiroaki et al. disclose a semiconductor device (fig. 1) comprising:

a wiring substrate 8;

an upper chip 14; and

a lower chip 10 or 12, the upper chip and the lower chip being mounted over an upper surface of the wiring substrate, and

wherein the upper chip is constructed as a multiport device including an interface between the upper chip and another part of the system including the lower chip and an interference between the upper chip and outside of the system,

wherein the lower chip is constructed to be accessed from the outside of the system via the upper chip,

wherein the upper chip 14 has a substantially square planar shape,

wherein the lower chip 10 or 12 has a substantially rectangular planar shape, with a long side having a greater length than a second side thereof adjacent to the long side,

wherein a length of a side of the upper chip 14 is shorter than a length of a long side of the lower chip, and

wherein the upper chip 14 is mounted over the wiring substrate 8 in as state being stacked over the lower chip 10 or 12,

wherein the upper chip 14 includes a first plurality of bonding terminals on an upper surface thereof, and the lower chip 12 includes a second plurality of bonding terminals on an upper surface thereof,

wherein the bonding terminals of the lower chip are disposed along the second side of the lower chip, and the bonding terminals of the upper chip 14 are disposed along a side of the upper chip 14 adjacent to the second side of the lower chip 12 (fig. 1, abstract).

Hiroaki et al. do not explicitly disclose the upper chip and lower chips are the microcomputer chip and the memory chip such that the microcomputer chip covers a portion of the long side of the memory chip and covers no portion of the side of the memory chip adjacent to the long side.

However, Katagiri et al. disclose a semiconductor device comprising:

a wiring substrate 1;

a microcomputer chip 2C (fig. 2, column 9, line 62); and

a memory chip 2A or 2B (fig. 2, column 7, line 47), the microcomputer chip and the memory chip being mounted over an upper surface of the wiring substrate, and wherein the microcomputer chip 2C has a substantially square planar shape (fig. 33),

wherein the memory chip 2A has a substantially rectangular planar shape, with a long side having a greater length than a second side thereof adjacent to the long side (fig. 33), wherein a length of a side of the microcomputer chip 2C is shorter than a length of a long side of the memory chip 2A (fig. 33), and

wherein the microcomputer chip 2C is mounted over the wiring substrate in as state being stacked over the memory chip such that the microcomputer chip covers a portion of the long side of the memory chip and covers no portion of the second side of the memory chip (fig. 2 and 33).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Hiroaki et al. by having the upper chip and lower chips are the microcomputer chip and the memory chip such that the microcomputer chip covers a portion of the long side of the memory chip and covers no portion of the side of the memory chip adjacent to the long side as taught by Katagiri et al. in order to provide a stacked multi-chip device that substantially enhances IC density (fig. 33) and also a technique which can reduce the cost of manufacturing a multi-chip module (column 2, lines 38-39).

Regarding claim 2, Hiroaki et al. discloses that the upper chip 14 is connected to first electrodes of said wiring substrate 8 via a plurality of bonding wires 19, the lower chip 10 or 12 is connected to second electrodes of said wiring substrate 8 via a plurality of bonding wires 17, said first electrodes are arranged toward an outer periphery side of said wiring substrate from the second electrodes (fig. 1).

Regarding claim 3, Katagiri et al. disclose that the memory chip includes a flash memory (column 7, line 47).

Regarding claim 7, Hiroaki et al. disclose that the upper chip 14 is connected to first electrode of the wiring substrate 8 via a plurality of bonding wires 19, a lower chip 10 of the two chips is connected to second electrodes of the wiring substrate 8 via a

plurality of bumps electrodes 9, the chip 12 is connected to third electrodes of the wiring substrate 8 via a plurality of bonding wires 17, the first electrodes are arranged toward an outer periphery of the wiring substrate from the second and third electrodes (fig. 1, abstract).

Regarding claim 8, Katagiri et al. disclose a semiconductor device comprising the memory chip includes a flash memory (column 7, line 47). It would have been obvious to one having ordinary skill in the art to form the lower chip 10 or 12 of Hiroaki et al. includes DRAM.

Regarding claim 9, Hiroaki et al. disclose a lower surface of the wiring substrate 8 is formed with a plurality of bump electrodes 22 constructing external connection terminals (fig. 1).

Regarding claim 10, Hiroaki et al. disclose the upper chip 14 and the lower chips 10 or 12 have respective terminals, and it would have been obvious to form a number of terminals of the upper chip being much greater than a number of terminals of the lower chips (fig. 1). Moreover, the number of terminals would have been obvious to an ordinary artisan practicing the invention because, absent evidence of disclosure of criticality for the number of terminals giving unexpected results, it is not inventive to discover number by routine experimentation. *In re Aller*, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). Furthermore, the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where patentability is aid to be based upon particular chosen number or upon another

variable recited in a claim, the Applicant must show that the chosen number is critical. See *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed, Cir. 1990).

Regarding claim 11, Hiroaki et al. disclose the terminals of the lower chips 10 or 12 are arranged such that they are not superposed over the terminals of the upper chip 14 in plan view (fig. 1).

Regarding claim 12, Hiroaki et al. disclose that an under fill resin 21 is filled in a gap between the lower chip 10 and the wiring substrate 8 (fig. 1).

Regarding claim 13, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have the two chips are arranged such that the long side of one of the chips crosses the long side of the other.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DILINH NGUYEN whose telephone number is (571)272-1712. The examiner can normally be reached on 8:00AM - 5:00PM (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DLN

/Theresa T. Doan/
Primary Examiner, Art Unit 2814